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JENNER & BLOCK, LLP			ARBES, CARL J	
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Please find below and/or attached an Office communication concerning this application or proceeding.



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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
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10/828,997	4/20/2004	DAVID W. CALDWELL	37041-11481
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EXAMINER

C. J. Arbes

ART UNIT

PAPER

3729

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Commissioner for Patents

On or about 28 July 2006 Applicants' attorney, Mark Vrlaⁱⁱⁱ, indicated that inasmuch as the Patent Office did use a Foreign Japanese Patent to reject certain ones of Applicants' claims and that the Patent Office had not provided an English translation of said foreign document would it be possible to obtain an English translation of said Japanese document. The Japanese Patent No in issue is: 030221922 by Y. Hatano et al. (The Patent inadvertently reversed the surname of the first named inventor with the given name). Accompanying this Memorandum please find the English translation of said Japan Pat No. 030221922.

The time period which was set in the former Non-Final Office Action (3 months) has not been extended by this Memorandum. FURTHERMORE the Patent Office Saith not.

C. J. Arbes
Primary Examiner
Art Unit: 3729

PTO 06-6145

CY=JA DATE=19910930 KIND=A
PN=03-221922

MANUFACTURING METHOD FOR DISPLAY DEVICE
[Hyoujisouchi no seizouhouhou]

Yuichi Hatano, et al.

UNITED STATES PATENT AND TRADEMARK OFFICE
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APPLICANT	(71):	JECO K.K.
TITLE	(54):	MANUFACTURING METHOD FOR DISPLAY DEVICE
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SPECIFICATION

1. Title of the Invention

MANUFACTURING METHOD FOR DISPLAY DEVICE

2. Claim

With respect to a display device equipped with a display part and a driving circuit part on the same transparent substrate, a display device manufacturing method characterized by forming conductor wirings by forming a film on a transparent substrate by doping a metal oxide with a noble metal, by forming a wiring pattern by patterning the film, and by subjecting the wiring pattern of only the driving circuit part to electroless plating.

3. Detailed Explanation of the Invention

[Industrial Field of Application]

The present invention relates to a manufacturing method for display devices, specifically to a manufacturing method for flat displays that are equipped with a display part and a driving circuit part on the same transparent substrate.

[Related Art]

In terms of a flat display equipped with a display part and a driving circuit part on the same transparent substrate, electroless plating is often carried out in order to form a conductor from a thin film on a driving circuit part obtained by patterning a transparent conductive film on a transparent substrate.

In the following, an electroless plating method commonly employed will be explained. It is impossible to directly perform electroless Ni plating on a driving circuit part that was formed by patterning a

transparent conductive film of ITO (indium tin oxide) or the like on a transparent substrate. Therefore, the process illustrated in Fig. 4 is carried out. In other words, after degreasing (Step 401) and conditioning (Step 402) the transparent conductive film patterned on a transparent substrate, sensitizing, in which SnCl_2 becomes attached, is carried out (Step 403). Furthermore, activating, in which Pd becomes deposited on the transparent conductive film through reaction, is carried out (Step 404). Next, electroless Ni plating (Step 405) is carried out by using this Pd as the nucleus. By then executing drying (Step 406), an Ni thin film becomes formed on the patterned transparent conductive film.

[Problems that the Invention is to Solve]

However, according to the above-described electroless Ni plating method, it takes a long time for the Pd nucleus to be formed on the patterned transparent conductive film. Moreover, selective formation of a Pd nucleus on the transparent conductive film involves many unstable factors, such as the management of the bath for the treatment solution, rinsing, etc. Moreover, Ni becomes deposited abnormally even on the transparent substrate, and there is a problem in that it short circuits the pattern of the driving circuit part.

[Means for Solving the Problem]

In order to solve such a problem, the present invention forms conductor wirings by forming a film on a transparent substrate by doping a metal oxide with a noble metal, by forming a wiring pattern by patterning the film, and by subjecting the wiring pattern of only the driving circuit part to electroless plating.

[Operation of the Invention]

According to the present invention, a catalytic nucleus becomes generated by doping a metal oxide with a noble metal, and a conductor wiring can be selectively and surely formed on only a wiring pattern by means of electroless plating.

[Embodiment of the Invention]

Figure 1 is a cross-sectional drawing that illustrates the structure of a display device which is for explaining one embodiment of the display device manufacturing method of the present invention. In the same figure, a common electrode [2a] and wiring patterns, [2b] ~ [2d], that consist of a transparent conductive film are formed from a display part [I] to a driving circuit part [II] on a transparent substrate [1] composed of a transparent glass plate. The light transmissivity of the glass substrate having the formation of the transparent conductive film needs to be at least 80%. In this case, these common electrode [2a] and wiring patterns, [2b] ~ [2d], are formed by doping an oxide, such as ITO, SnO_2 , In_2O_3 , or ZnO, with a small amount of a noble metal, such as Pd, Au, Ag, or Pt, and by sputtering it onto the transparent substrate [1] or by carrying out electron beam evaporation, and the display part [I] and the driving circuit part [II] are provided with predetermined patterns by means of photolithography. Moreover, the wiring patterns, [2b] ~ [2d], that form the driving circuit part [II] of the transparent substrate [1] and that consists of the transparent conductive film have formed on them an electroless nickel plated layer [3], which forms conductor wirings, [4a], [4b], and [4c]. An IC chip [5] and a chip component [6] are packaged between

these conductor wirings, [4a], [4b], and [4c], in an electrically connected manner by means of soldering. Incidentally, a liquid-crystal oriented film [7] is formed on the common electrode [2a], which consists of the transparent conductive film of the display part [I] side, and an electrode substrate [10], in which a display electrode [9] and a liquid-crystal oriented film [8] are formed on the opposing face of a front substrate [8] that consists of a translucent glass plate, is adhered by a sealing member [11] and is disposed in an opposing manner. A TN crystal liquid [12], for example, is sealed between these opposing components.

For this structure, the conductor wirings, [4a], [4b], and [4c], are formed on the driving circuit part [II] of the transparent substrate [1] by first forming the transparent conductive film [2] on the transparent substrate [1] by doping a metal oxide, such as ITO, SnO_2 , In_2O_3 , or ZnO , with a small amount of a noble metal, such as Pd, Au, Ag, or Pt, by means of sputtering or the electron beam evaporation method and by then forming the common electrode [2a] and the wiring patterns, [2b] ~ [2d], by carrying out, for example, etching. In this case, the wiring patterns, [2b] ~ [2d], are formed as microscopic patterns that have wiring widths of about 20 through $30\mu\text{m}$. Next, as indicated in the flow chart of Fig. 2, the transparent substrate [1] having the formations of these common electrode [2a] and wiring patterns, [2b] ~ [2d], is degreased (Step 201) for 3 minutes at about 50°C by using, for example, an ITO cleaner (made by Okuno Chemical Industries Co., Ltd.), is rinsed with water, and then becomes conditioned (Step 202) by being immersed in, for example, a 1% sulfuric acid solution for about 1.5 minutes at room temperature. Then, after being rinsed with

water, the display part [I] side on the transparent substrate [1] becomes masked, and an electroless nickel plating layer [3] that is about 2 μ m in thickness is formed on the wiring patterns, [2b] ~ [2d], of the driving circuit part [II] side by performing electroless nickel plating (Step 203) with, for example, Ni-B-series ITO-70 (made by Okuno Chemical Industries Co., Ltd.) at 83°C or Ni-B-series SS-55-1 (made by Okuno Chemical Industries Co., Ltd.) at 63°C (made by Japan Kanigen Co., Ltd.). Then, after being rinsed with water and then dried (Step 204), it becomes completed by having formed on it the conductor wirings, [4a], [4b], and [4c].

According to this method of forming the conductor wirings, [4a] ~ [4c], the wiring patterns, [2b] ~ [2d], consisting of the transparent conductive film are formed on the transparent substrate [1] by doping the metal oxide with a small amount of a noble metal, and the electroless nickel plating layer [3] is then formed on these wiring patterns, [2b] ~ [2d]. By this, the noble metal that the wiring patterns, [2b] ~ [2d], are doped with acts as a catalytic nucleus, allowing the electroless nickel plating layer [3] to be formed selectively and surely on only the wiring patterns, [2b] ~ [2d], by means of electroless nickel plating. Therefore, it can be formed at microscopic line pitches that do not cause short circuit between the mutually-adjacent conductor wirings, [4a], [4b], and [4c], and can also be formed in a simple process.

Furthermore, according to this method of forming the conductor wirings, [4a] ~ [4c], it is possible to dispose the display part [1] at the center of the transparent substrate and to package multiple IC chips

[5] and chip components [6] around it. Also, by sealing at least one portion by means of an insulating resin [13], it becomes possible to realize a flat display in which the display part [I] and the driving circuit part are integrally formed on the same substrate.

Moreover, a case in which a liquid-crystal display device is the display device was explained in the above-described embodiment, but the present invention is not limited to this and can also be applied to flat displays such as a PDD (plasma display), ECD (electrochromic display), and EL (electroluminescence).

[Effects of the Invention]

As explained earlier, according to the present invention, the conductor wirings of the driving circuit part formed on the transparent substrate are obtained by forming a film by doping a metal oxide with a noble metal, by patterning it, and by then subjecting it to electroless plating. Therefore, superb effects can be achieved in that the conductor wirings can be formed selectively and surely at microscopic line pitches in a simple process.

4. Brief Explanation of the Drawings

Figure 1 is a cross-sectional drawing of the essential part of a display device that is for explaining one embodiment of the display device manufacturing method of the present invention, Figure 2 is a flow chart of the manufacturing process thereof, Figure 3 is a perspective drawing showing the structure of a flat display, and Figure 4 is a flow chart of a conventional manufacturing method.

[1] = transparent substrate; [2a] = common electrode; [2b], [2c], [2d] = wiring pattern; [3] = electroless nickel plating layer; [4a], [4b], [4c] = conductor wiring; [5] = IC chip; [6] = chip component; [7] = liquid-crystal oriented film; [8] = front substrate; [9] = display electrode; [10] = electrode substrate; [11] = sealing member; [12] = TN liquid crystal; [13] = insulating resin.

Figure 1

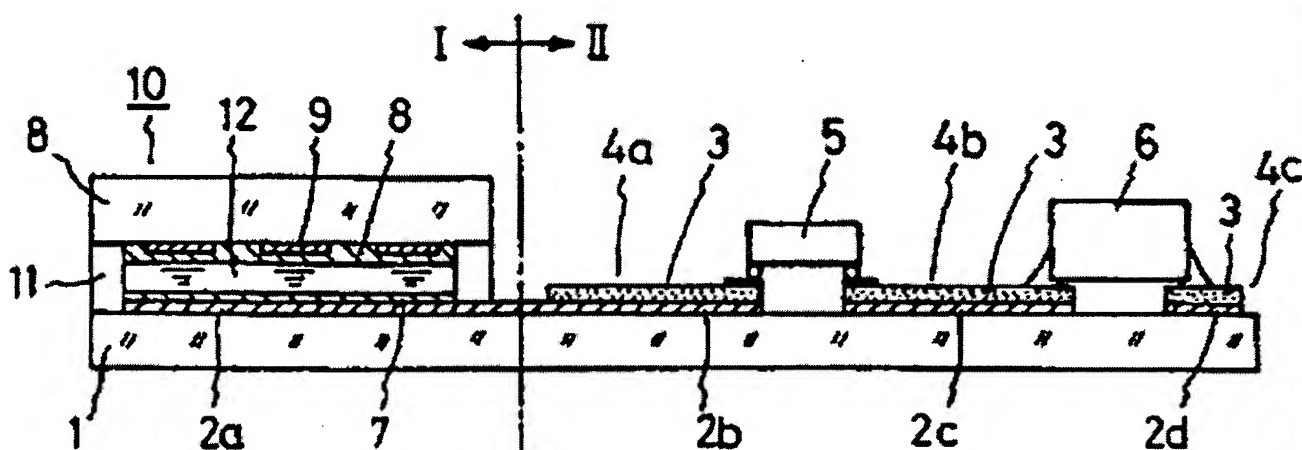


Figure 2

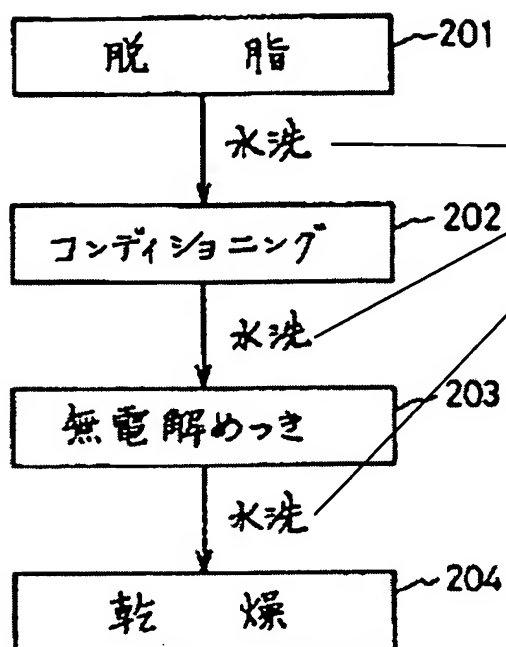
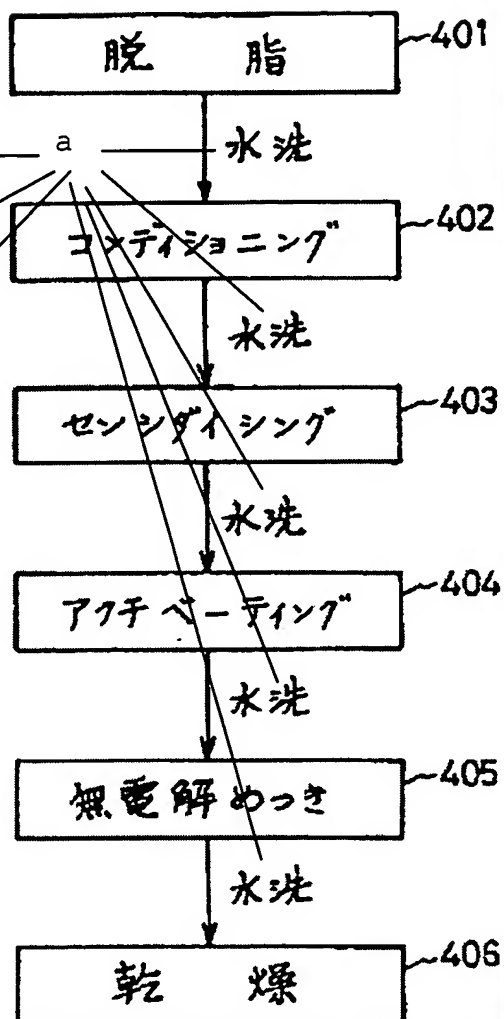


Figure 4



Key: 201,401)degreasing; 202,402)conditioning; 203,405)electroless plating; 204,406)drying; 403)sensitizing; 404)activating; a)rinsing.

Figure 3

